ABSTRACT OF THE DISCLOSURE

In a shift clock signal generating apparatus, a delay line includes a plurality of unit delay elements connected in cascade. A reference clock signal propagates in the delay line while being successively delayed by the unit delay elements. Switches have first ends connected with output terminals of the unit delay elements respectively, and second ends connected with a shift clock signal output path. When specified one among the switches is in its on position, a delayed clock signal which results from delaying the reference clock signal by a prescribed time interval is transmitted via the specified switch to the shift clock signal output path as a shift clock signal. The specified one among the switches is determined on the basis of data representing a phase difference of the shift clock signal from the reference clock signal. The specified switch is set in its on position.